CMOS Image Sensors with High Quantum Efficiency

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Summary

We aim to develop the next generation of CMOS image sensors suitable for Earth observation, ground and space-based astronomy, and other science applications requiring high QE in the red and near-infrared parts of the spectrum. The main innovation is the achievement of high QE by full depletion of the thick sensitive semiconductor layer using reverse substrate bias. In this way sensitive detector thickness of 100 µm or more can be realised, instead of the current 5-10 µm thick devices. The development will concentrate on building silicon CMOS image sensors using pinned photodiode photosensitive elements, capable of achieving science-grade imaging performance.

The technological advances from this work will allow many space-based imaging instruments to transition from CCD to CMOS devices and benefit from better radiation hardness, higher readout speeds, increased level of integration and lower power dissipation.

CMOS image sensors

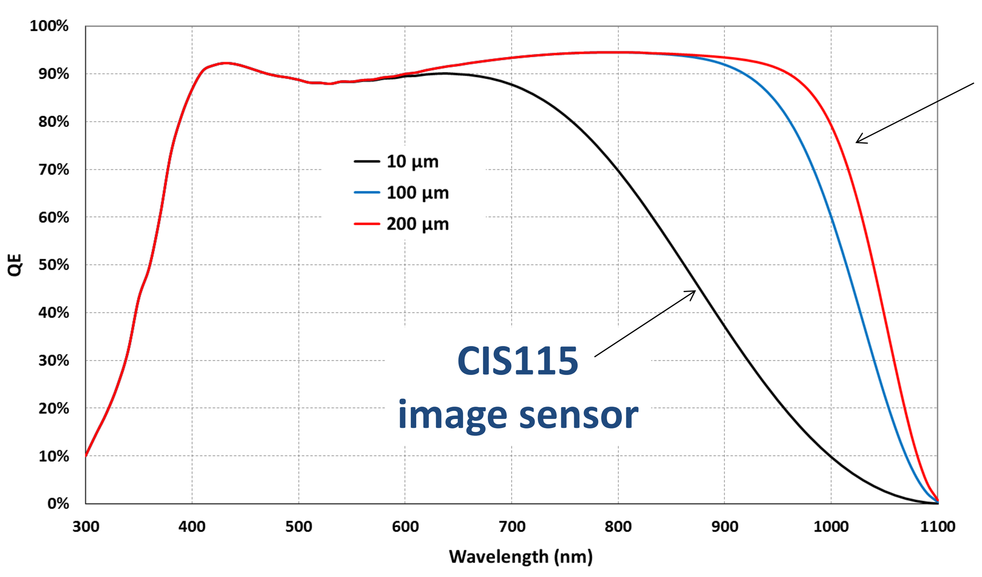
Scientific and space applications of CMOS image sensors (CIS) are increasing thanks to their constantly improving performance. For consumer imaging CIS are dominating.

For space CIS offer better radiation hardness due to the use of thinner dielectrics and minimal number of charge transfers. Low power consumption is also a significant advantage.

CIS offer higher level of system integration as ADCs and image processing can be placed on the same chip, resulting in higher overall system integration and reliability.

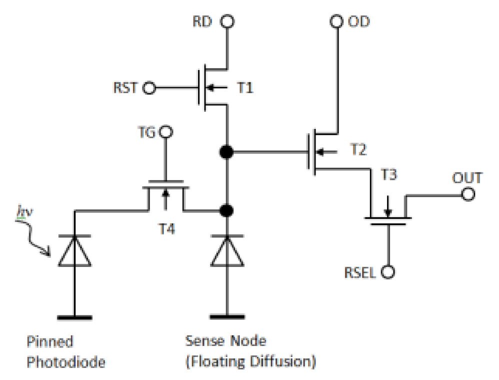
Back side illumination (BSI) is now routinely available, significantly improving the sensor Quantum Efficiency (QE).

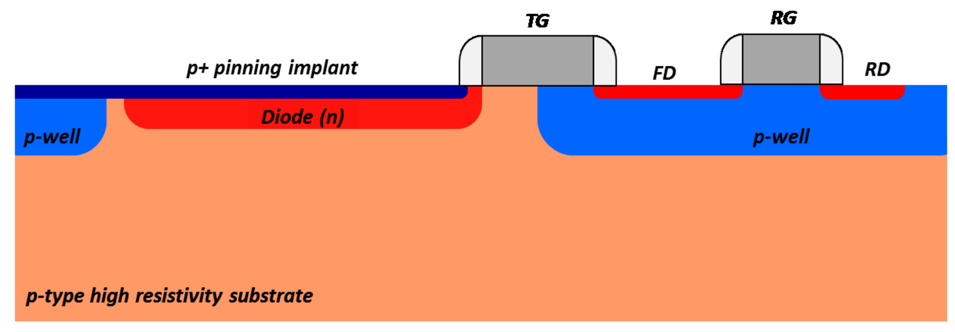
However, the QE of CIS is not competitive with CCDs at near-IR wavelengths because the sensitive depleted region rarely exceeds 10 µm even in BSI devices, compared to thicknesses of greater than 100 µm with state-of-the-art BSI CCDs.



Higher QE when deeper depletion is achieved – the goal of this development.

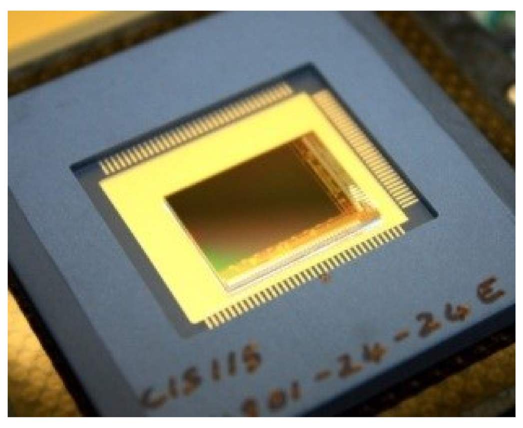
Pinned photodiode technology





Pinned photodiode (PPD, or 4T) is the preferred photosensitive element in modern CMOS image sensors. It has excellent imaging performance due to:

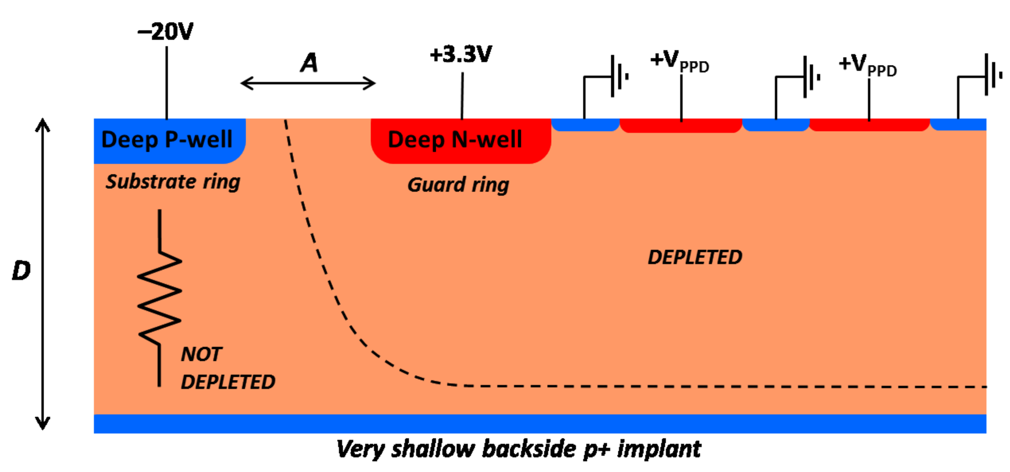
- Low readout noise with correlated double sampling inherently built-in. Readout noise below 1 e- RMS is not unusual.
- Sensitivity in excess of 100 µV/e- is routinely achieved.
- Photodiode in not covered by a gate and QE for front illumination is very good.
- Very low dark current due to surface pinning, on a par with the best CCDs.



Example: CIS115 CMOS Image Sensor

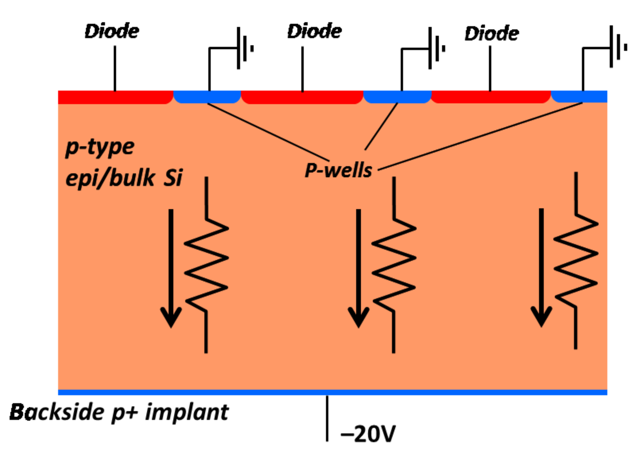
- To be used in the JANUS visible camera on board the ESA JUICE spacecraft to Jupiter
- Designed by e2v Technologies (UK)
- 2000 (V) × 1504 (H) image format
- 7 µm square pixels using PPD

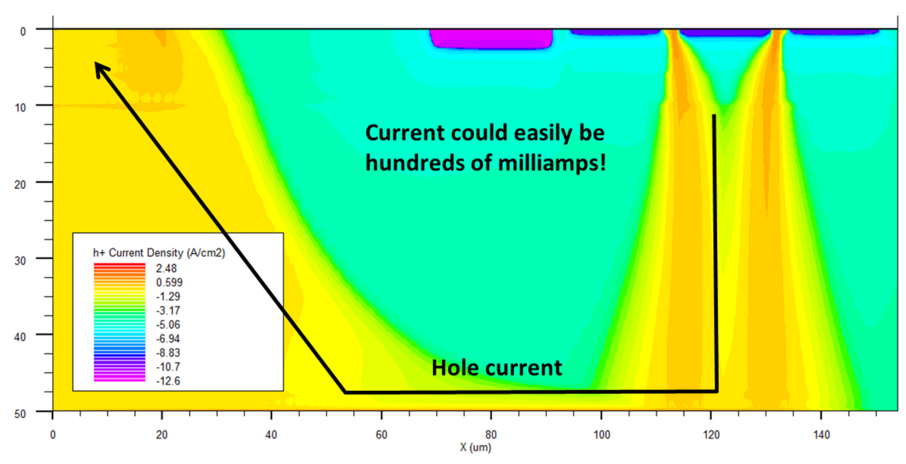
Increasing the depleted thickness via reverse substrate bias



Typical bias voltages in CIS do not exceed 3.3V, and this is not enough to deplete more than about 10 µm even in high resistivity substrates. Significant increase of the depletion depth is possible with reverse substrate bias, which can be much higher than the normal operating voltages in CIS.

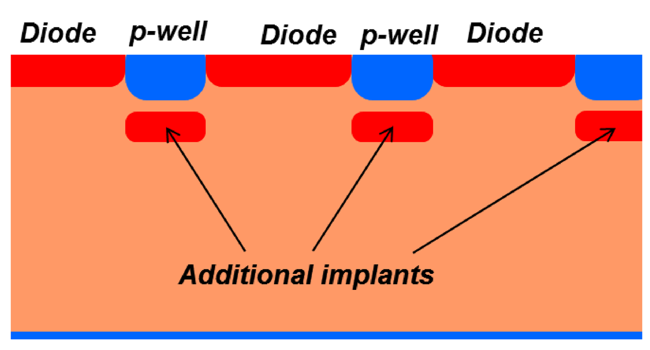
The reverse biasing concept is borrowed from CCDs, where all voltages are applied from the front. However, the presence of front-side p-wells in CIS makes backside biasing much more difficult. Parasitic conductive p+/p/p+ path is formed between the front and the back of the device, which prevents practical use. A new concept is required to allow reverse biasing while keeping the CIS PPD circuitry unchanged.





Present work

We are proposing a method to reverse bias a PPD image sensor while suppressing the parasitic substrate current. The successful development is expected to underpin wide array of new instrumentation from near-infrared to soft X-ray wavelengths, and will benefit EO, astronomy and many other areas of science and technology.

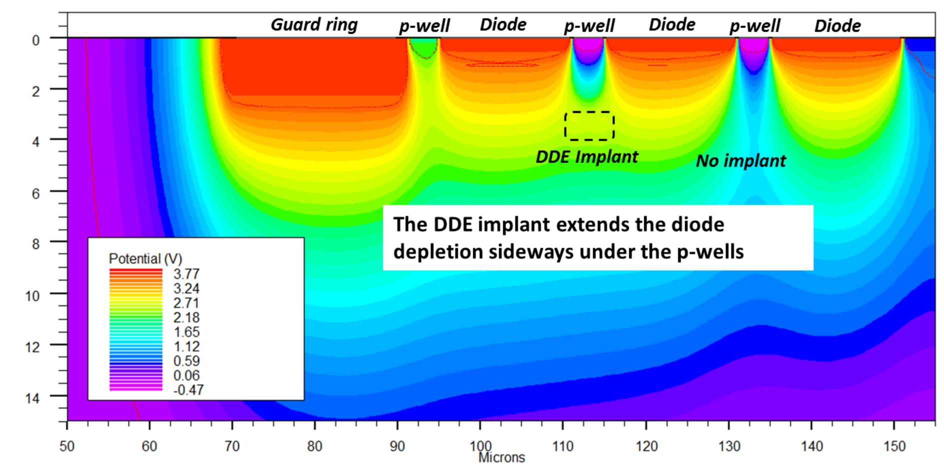


Additional deep n-type implants are placed under the p-wells. This draws in the depletion sideways from the PPDs under the p-wells, achieving pinch-off. The front-to-back current is suppressed by a potential barrier.

A patent application has been filed.

This method has a number of advantages:

- The excellent properties of the PPD are preserved, as it remains unchanged.
- The structure is compatible with any depleted thickness.
- Only one additional manufacturing step is required.



This project is funded by the NSTP-2 call from CEOI-ST and started in February 2015.

Presently working with TowerJazz Semiconductor to design and manufacture a prototype device, in collaboration with e2v Technologies.

The Open University

CEOI Technology Conference

21-22 April 2015

Centre for Electronic Imaging

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